EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	199	703/2.ccls. and @pd>"20070601"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/11/26 18:41

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S11	602	hdl and $7.v and @ad<"20011201"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/11/26 13:47
S12	59	hdl and (parameter adj file) and @ad<"20011201"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/11/26 14:11
S13	14	hdl and (define adj file) and @ad<"20011201"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/11/26 14:25

Google Scholar BETA

Web Images Video News Maps more »

hdl parameter file 1990 - 2001 Search Ad Sc Sc

Scholar **All articles - Recent articles** Results **1 - 10** of about **1,180** for **hdl parameter file**. (**0.16** seco

All Results
K Hayes
P Ridker
D Wingard
G Redden
W Ela

Method and apparatus for efficiently implementing complex function blocks in integrated circuit ... - all 3 versions »
KA Dockser, GE Ehmann... - US Patent 5,963,454, 1999 - Google Patents
... As such, the **parameter file** includes information used to define global **parameters** for the **HDL** template with which the **parameter file** is associated. ...
Cited by 15 - Related Articles - Web Search

Functional verification methodology for the PowerPC 604 microprocessor - all 3 versions »
J Monaco, D Holloway, R Raina - Proceedings of the 33rd annual conference on Design ..., 1996 - portal.acm.org
... hardware design modeling language (**HDL**) now entrenched ... verification engineer specified
a **file** containing one ... These biasing **parameter files** were referred to as ...
Cited by 42 - Related Articles - Web Search

Hardware/software co-simulation in a VHDL-based test bench approach - all 12 versions »
M Bauer, W Ecker - Proc. of the Design Automation Conference, 1997 - doi.ieeecomputersociety.org
... VHDL design units, which we call in this case applications, relate ... techniques are also supported eg by a **file** name associated as a **parameter** with an ...
Cited by 18 - Related Articles - Web Search

Method and apparatus for generating optimized functional macros - all 2 versions »
GR Goslin, BC Thielges, SH Kelem - US Patent 6,120,549, 2000 - Google Patents
... for From elaborated VHDL module 404 symbol **file** 408 is **parameter** A of 10 and a value for **parameter** B of 10. Area also generated. ...
Cited by 11 - Related Articles - Web Search

VHDL & Verilog Compared & Contrasted-Plus Modeled Example Written in VHDL, Verilog and C. - all 13 versions »
DJ Smith - Proc. 33rd Design Automation Conf, 1996 - doi.ieeecomputersociety.org
... be placed in a separate system **file** and included ... to parameterize models by overloading **parameter** constants, there is ... to the high-level VHDL modeling statements ...
Cited by 26 - Related Articles - Web Search

Surface complexation models: An evaluation of model **parameter** estimation using FITEQL and oxide ... - all 2 versions »
KF Hayes, G Redden, W Ela, JO Leckie - Journal of Colloid and Interface Science, 1991 - deepblue.lib.umich.edu
... URL to cite or link to this item: http://**hdl**.handle.net ... A method is suggested for choosing a unique set of **parameter** values for ... **File**, Description, Size, Format, ...
Cited by 98 - Related Articles - Cached - Web Search

Self-Test Methodology for At-Speed Test of Crosstalk in Chip Interconnects -

Results for "((hdl<and>parameter file)) <and> (pyr >= 1913 <and> pyr <= 2001)"
Your search matched **3** of **1690033** documents.
A maximum of **250** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

Modify Search

((hdl<and>parameter file)) <and> (pyr >= 1913 <and> pyr <= 2001) Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Search Options

View Session History

New Search

» Key

	Indicates full text access
IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

IEEE/IET Books Educational Courses A

Interactive online content developed from IEEE conference tutorials.

view selected items Select All Deselect All

1. **A general purpose simulation environment for HDL based verification**
   Rajadnya, S.; Palnitkar, A.;
   Verilog HDL Conference, 1997., IEEE International
   31 March-2 April 1997 Page(s):14 - 21
   Digital Object Identifier 10.1109/IVC.1997.588527
   Abstract | Full Text: PDF(788 KB) IEEE CNF
   Rights and Permissions

2. **Self-test methodology for at-speed test of crosstalk in chip interconnect**
   Xiaoliang Bai; Dey, S.; Rajski, J.;
   Design Automation Conference, 2000. Proceedings 2000. 37th
   June 5-9, 2000 Page(s):619 - 624
   Abstract | Full Text: PDF(632 KB) IEEE CNF
   Rights and Permissions

3. **Designing ASICs with UAHPL**
   Sait, S.M.; Benten, M.S.T.; Khan, A.M.T.;
   Circuits and Devices Magazine, IEEE
   Volume 11, Issue 2, March 1995 Page(s):14 - 24
   Digital Object Identifier 10.1109/101.366091
   Abstract | Full Text: PDF(972 KB) IEEE JNL
   Rights and Permissions